DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

IN THE CLAIMS

(APPLICATION PAGES 14-16)

Before claim 1, change "**Patent Claims**" to --WE CLAIM:--

Please amend claims 1-12 as follows:

1. (amended) A method for modulating a basic clock signal for digital circuits, in which [the] distances between adjacent switching edges are altered, the basic clock signal being conducted via a changing number of delay units and the distances between the adjacent switching edges being altered in this way, [**wherein** the] comprising the step of calibrating delay times of the delay units (D1-Dn) [are calibrated], wherein the delay units (D1-Dn) each have a plurality of delay elements (10) which are connected in or out individually and/or in groups.

2. (amended) The method as claimed in claim 1, **wherein**, ~~in order to calibrate~~ the delay units (D1-D7), ~~the method~~ comprises the step of connecting the delay elements (10) [are connected] in or out in a stepwise approximated manner.

3. (amended) The method as claimed in claim 2, **wherein**, ~~firstly,~~ during a coarse calibration, [the] a same number of delay elements (10) is connected in or out in each case in all the delay units (D1-D7) and then, in a fine calibration, a respective delay element (10) in one or more delay units (D1-D7) is connected in or out.

4. (amended) The method as claimed in claim 2, **wherein**, in a series of delay units (D1-D4) which extends from the first delay unit (D1) up to the delay unit (D4), at [whose] an output of which the clock signal is delayed by half a period given a correct delay, during a coarse calibration, [the] a same number of delay elements (10) is connected in or out in each case in all the delay units (D1-D4) and then, in a fine calibration, a respective delay element (10) in one or more delay units (D1-D4) is connected ~~in~~ or out until, at the output of the ~~last~~ delay unit (D4) of the series, the clock signal is delayed by half a period, wherein the remaining delay units (D5-D7) are subsequently set in a corresponding manner.

5. (amended) The method as claimed in claim 1 [one of the preceding claims], **wherein** the respective distance between two adjacent switching edges is derived from numbers of a random number generator.

6. (amended) The method as claimed in claim 5, **wherein** [the] said random number generator generates cyclically recurring random numbers.

7. (amended) The method as claimed in claim 6, **wherein** the random numbers are inverted after n cycles for n cycles and the method further comprising the step of using these inverted random numbers [are used] for deriving the adjacent switching edges.

8. (amended) The method as claimed in claim 5 [one of the preceding claims], **wherein** the distance between two successive switching edges is derived as a function of the random number and a modulation factor.

9. (amended) The method as claimed in claim 8, [**wherein**] further comprising the step of calculating the position of a switching edge (a_{i+1}) succeeding a switching edge (a_i) [is calculated] as follows:

$$a_{i+1} = \left(a_i + p - \left(\frac{N-1}{2} - Z_{i+1} \right) K \right) \bmod p$$

where

p represents the number of delay steps per half-period,

N represents the number of possible switching edges,

K represents the modulation factor, and

Z represents the random number.

10. (amended) A clock modulator having a number of delay units connected in series, taps being arranged between the delay units and the basic clock signal being [able to be conducted] conductable via a changing number of delay units and the distance between the switching edges being [able to be altered] alterable in this way, for implementing the method as claimed in claim 1 [one of the preceding claims], **wherein** [the] delay times of the delay units are adjustable and calibratable, the delay units having series-connected delay elements which [can be connected] are connectable in and [disconnected] disconnectable individually.

11. (amended) The clock modulator as claimed in claim 10 further comprising a random number generator, **wherein** cyclically recurring random numbers [can be generated] are generatable by said random number generator, and wherein the distances between adjacent switching edges [can be derived] are derivable from the random numbers.

12. (amended) The clock modulator as claimed in claim 11, further comprising [**wherein**] an inverting device for inverting the random numbers [is present], wherein the inverting device is connectable [can be connected] in after n cycles and [can be disconnected] is disconnectable again after a